REMARKS

Claims 3-7 and 9-29 were previously pending in this application. No new claims have been added and no amendments are submitted herewith. As a result claims 3-7 and 9-29 are pending for examination with claims 11, 15 and 24 being independent claims.

Summary of Telephone Conference with Examiner

Applicants thank Examiner Vent for her time and courtesy during the telephone interview conducted on June 26, 2007 with inventor Andre Laframboise and Meriem Debbih of Matrox Electronic Systems, and the undersigned. During the interview Mr. Laframboise provided background concerning the state of the art in video processing and graphics accelerators at the time of the invention. In addition, Mr. Laframboise discussed the subject matter of the cited references U.S. Patent No. 6,678,002 to Frink et al. (hereinafter "Frink") and U.S. Patent No. 6,853,385 to MacInnis et al. (hereinafter "MacInnis"). Mr. Laframboise explained that Frink and MacInnis employ graphics accelerators in their traditional role at the time of the invention, for example, to generate graphics data for inclusion in a video image (e.g., text appearing in a video image). Mr. Laframboise further explained that neither Frink nor MacInnis employed a graphics accelerator to edit at least two real-time uncompressed digital video streams and provide a video output that included the edited video as recited in claim 24. Accordingly, neither Frink nor MacInnis describe that a graphics accelerator includes at least two video inputs for receiving at least two real-time uncompressed digital video streams. At the conclusion of the discussion, Examiner Vent indicated that the Applicants had overcome the art of record in view of the explanation provided by Mr. Laframboise. Examiner Vent also stated that further search and examination were required.

Rejections Under 35 U.S.C. §103

The Office Action rejects claims 3-7 and 9-29 under 35 U.S.C. §103(a) as being unpatentable over Frink in view of MacInnis. As indicated above, Applicants respectfully disagree because neither Frink nor MacInnis perform any video editing operations on real time uncompressed digital video streams.

Regarding Frink, the Office Action indicates that col. 10 lines 40+ and Fig. 5 describes "the input of two uncompressed digital video streams that are used for editing uncompressed video and then providing the input back to the system." (Office Action at page 9.) Applicants respectfully disagree, at least, because Frink does not teach or suggest that a graphics accelerator has any video editing functionality let alone how a graphics accelerator can be employed to edit any real-time uncompressed video. Instead of performing video editing functions, the graphics accelerator 552 taught by Frink merely provides video with graphics data in the form of "static titles" and animated graphics. (Col. 10, lines 39-49.) Frink does not teach or suggest that a graphics accelerator can employ "a 2D graphics engine and a 3D rendering engine respectively for providing 2D and 3D functions used for said video editing" of a single video input let alone that the graphics accelerator 552 can perform such editing on "two real-time uncompressed digital video streams" as recited in claims 11 and 24. (Emphasis added.) That is, Frink employs a graphics accelerator in a traditional manner to generate graphics and combine the graphics with the video. Graphics data and video are very different image formats. As a result, processing graphics data and combining it with video is nothing like employing the 2D graphics engine and the 3D rendering engine of the graphics accelerator (which is designed to manipulate graphics data) to perform video editing of at least two real-time uncompressed digital video streams. Frink fails to address such a possibility. Further, Frink expressly indicates that video editing is performed elsewhere in the system, namely in the HD DVE module 554 and the HDTV 3D DVE module 550. (See col. 10, lines 30-39, describing that 3D digital video effects, compositing, etc. are performed in the modules 554 and 550.)

The Office Action also indicates that "Frink et al shows in Figure 5 a graphic accelerator chip with two inputs of uncompressed digital video." (Office Action at page 2.) Applicants respectfully disagree and assert that such an interpretation of Figure 5 is inaccurate and inconsistent with the teachings of Frink. As described above, Frink describes that a graphics accelerator 552 may combine video with graphics and indicates that video editing operations including 3D video effects are performed elsewhere in the system. Accordingly, Applicants respectfully assert that a closer review of Fig. 5 which is fully consistent with the remainder of Frink finds that graphics and video are provided to the graphics accelerator 552 from the module

520 and that video and key are communicated from the graphics accelerator 552 back to the module 520. Accordingly, Frink also fails to teach or suggest "a graphics accelerator chip having at least two video inputs for respectively receiving at least two real-time uncompressed digital video streams" as recited in claims 11 and 24.

Regarding MacInnis, the Office Action indicates that Fig. 1, col. 5, lines 35+ and col. 60, lines 1-30 disclose "a graphics processing system [having at least] two video inputs receiving real-time uncompressed video streams" including "a 2D graphics engine and a 3D rendering engine respectively for providing 2D and 3D function of the uncompressed digital video streams." (Office Action at page 5.) Applicants respectfully disagree because MacInnis describes a system in which video and graphics are processed in separate processing pipelines before being combined in a compositor 108. (See Fig. 4.) That is, MacInnis employs "a dedicated processor" that includes "a memory for graphics data including pixels, and a coprocessor for performing vector type operations on a plurality of components of one pixel of graphics data." (Col. 59, lines 60-67, emphasis added.) As further explained in col. 60, "a graphics accelerator 64 receives commands from a CPU 22 and receives graphics data from main memory 28 through a memory controller 54." (Col. 60, lines 26-28, emphasis added.) As described above, graphics data and video are very different image formats. MacInnis fails to teach or suggest that any real-time uncompressed video streams are supplied to a graphics accelerator let alone that at least two real-time uncompressed digital video streams are supplied to a graphics accelerator. Thus, the graphics accelerator 64 taught by MacInnis operates on graphics data – not video.

MacInnis dedicates approximately three columns to a description of the graphics accelerator 64 and its operation. (Col. 59, line 55 through col. 62, line 54.) In this substantial description, MacInnis does not provide any teaching or suggestion that the graphics accelerator 64 even receives a real time uncompressed video stream. The vague and ambiguous use of terms such as "video surfaces," "video warping" and "video operations," that appear at col. 60, lines 1-17, does not change the fact that the entire disclosure, including the portion dedicated to a description of the graphics accelerator 64, fails to teach or suggest that the graphics accelerator actually receives real-time uncompressed video. Instead, MacInnis describes that the system

includes a "graphics display pipeline 80" and a separate "video display pipeline 82." (Col. 8, lines 30-32 and Fig. 4.) Accordingly, one of ordinary skill in the art would find that MacInnis employs a graphics processor to operate solely on graphics data and that col. 60, lines 1-17 refers solely to operations performed on graphics data – not video. Thus, MacInnis fails to teach or suggest either "a graphics accelerator chip having at least two video inputs for respectively receiving at least two real-time uncompressed digital video streams" or "a 2D graphics engine and a 3D rendering engine respectively for providing 2D and 3D functions used for said video editing," as recited in claims 11 and 24. (Emphasis added.)

For all of the above reasons, Applicants respectfully assert that neither Frink nor MacInnis alone or in proper combination teach or suggest all the limitations recited in independent claims 11 and 24. Neither Frink nor MacInnis either alone or in proper combination teach or suggest "a graphics accelerator chip having at least two video inputs for respectively receiving at least two real-time uncompressed digital video streams," as recited in claims 11 and 24. Further, neither Frink nor MacInnis alone or in proper combination teach or suggest the "graphics accelerator chip further having a 2D graphics engine and a 3D rendering engine respectively for providing 2D and 3D functions used for said video editing of said at least two real-time uncompressed digital video streams," as recited in claims 11 and 24. (Emphasis added.) Thus, independent claims 11 and 24 are patentable in view of the combination of Frink and MacInnis. Each of claims 3-7, 9, 10, 12-14 and 25-29 depend from one of claims 11 and 24 and are also patentable for the reasons described above.

In addition, neither Frink nor MacInnis alone or in proper combination teach or suggest all the limitations recited in independent claim 15. In particular, Frink and MacInnis alone or in proper combination do not teach or suggest "[a] method of editing a plurality of video streams with a graphics accelerator chip that includes a 2D graphics engine and a 3D rendering engine," that a graphics accelerator receives each of a first real-time uncompressed digital video stream and a second real-time uncompressed digital video stream or that the graphics accelerator "perform[s] video editing on the first real-time uncompressed digital video stream and the second real-time uncompressed digital video stream using the 2D graphics engine and the 3D rendering engine," as recited in claim 15. (Emphasis added.) Thus, independent claim 15 is

patentable in view of the combination of Frink and MacInnis. Further, each of claims 16-23 depend from 15 and are also patentable for the reasons described above.

Accordingly, reconsideration and withdrawal of the rejections of claims 3-7 and 9-29 is respectfully requested.

CONCLUSION

In view of the foregoing amendments and remarks, reconsideration is respectfully requested. This application should now be in condition for allowance; a notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed payment, please charge any deficiency to Deposit Account No. 50/2762, M1073-700719.

Respectfully submitted,
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